DERWENT-ACC-NO: 1988-141950

DERWENT-WEEK: 198821

TITLE: IC testing system which uses generated vectors - uses processor to determine test vectors which are modified using maximum number of possible faults

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PRIORITY-DATA: 1986FR-0014148 (October 10, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 268506 A	May 25, 1988	F	032	N/A
FR 2605112 A	April 15, 1988	N/A	000	N/A
US 5010552 A	April 23, 1991	N/A	000	N/A

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APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 268506A	N/A	1987EP-0402217	October 6, 1987
FR 2605112A	N/A	1986FR-0014148	October 10, 1986
US 5010552A	N/A	1987US-0107502	October 8, 1987

INT-CL (IPC): G01R031/28, G06F011/22

ABSTRACTED-PUB-NO: EP 268506A

BASIC-ABSTRACT:

The system uses a processor (72) linked to a memory (71) in which the characteristics of the test IC (70) are entered. These characteristics are used by the processor (72) to allow all possible circuit faults to be determined and fed to a test vector generator supplying the test vectors to a circuit testing device (75).

The processor is used to determine the test vectors which are modified by the max. number of possible faults. This allows the min. number of test vectors to be used to detect all possible circuit faults.

USE - For adaptable testing of programmable logic array.

ABSTRACTED-PUB-NO: US 5010552A

EQUIVALENT-ABSTRACTS:

The device used to test integrated circuits has possible faults of a circuit to be tested determined including logic faults caused by the physical structure and relative position of the circuit elements in the integrated logic circuit.
On the basis of the faults, a set of test vectors is determined, each fault modifying at least one of the test vectors applied to the circuit to be tested.
It is possible to use test vectors which are modified by the greatest number of possible faults. By determining the test vectors on the basis of the faults which are to be detected, the tests can use a small number of vectors while, at the same time, there is certainty that it will be possible to detect all the faults in a given circuit. A hierarchially-organised set of cells is determined with certain cells consisting of small cells.

USE - To test PLAs
using small number of test vectors. (28pp)

CHOSEN-DRAWING: Dwg.53/54

TITLE-TERMS: IC TEST SYSTEM GENERATE VECTOR PROCESSOR
DETERMINE TEST VECTOR
MODIFIED MAXIMUM NUMBER POSSIBILITY FAULT

DERWENT-CLASS: S01 T01 U11 U13 U21

EPI-CODES: S01-D01A; S01-G02; T01-G02; U11-F01C3;
U11-F01C5; U13-C04C;
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